

Lab Report - 02

Course No: 206

Course Title: Digital Logic Design

**Submitted To:**

Iffat Tamanna

Dept: CSE

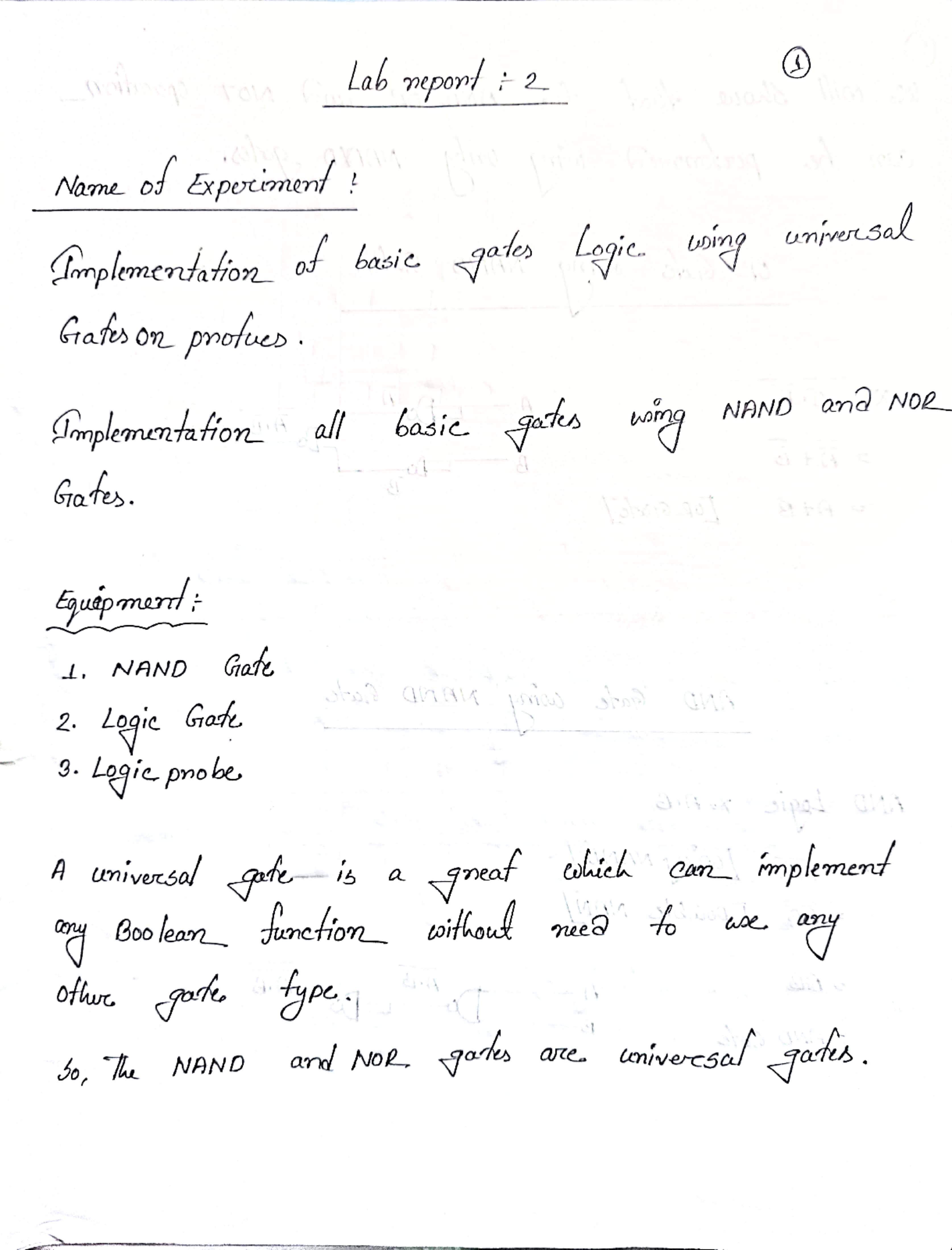
**Submitted By:**

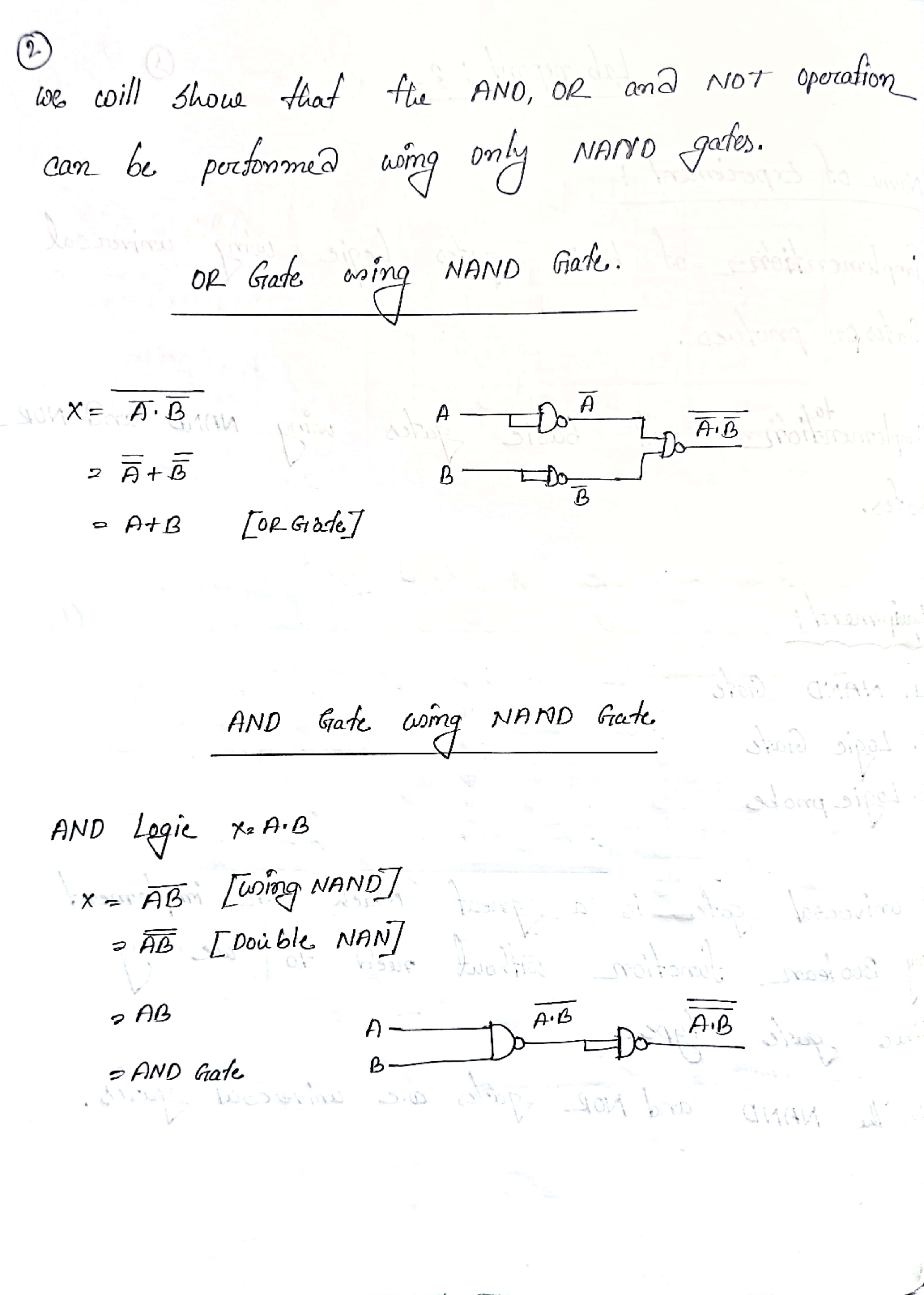
Md: Zobayer Hasan Nayem

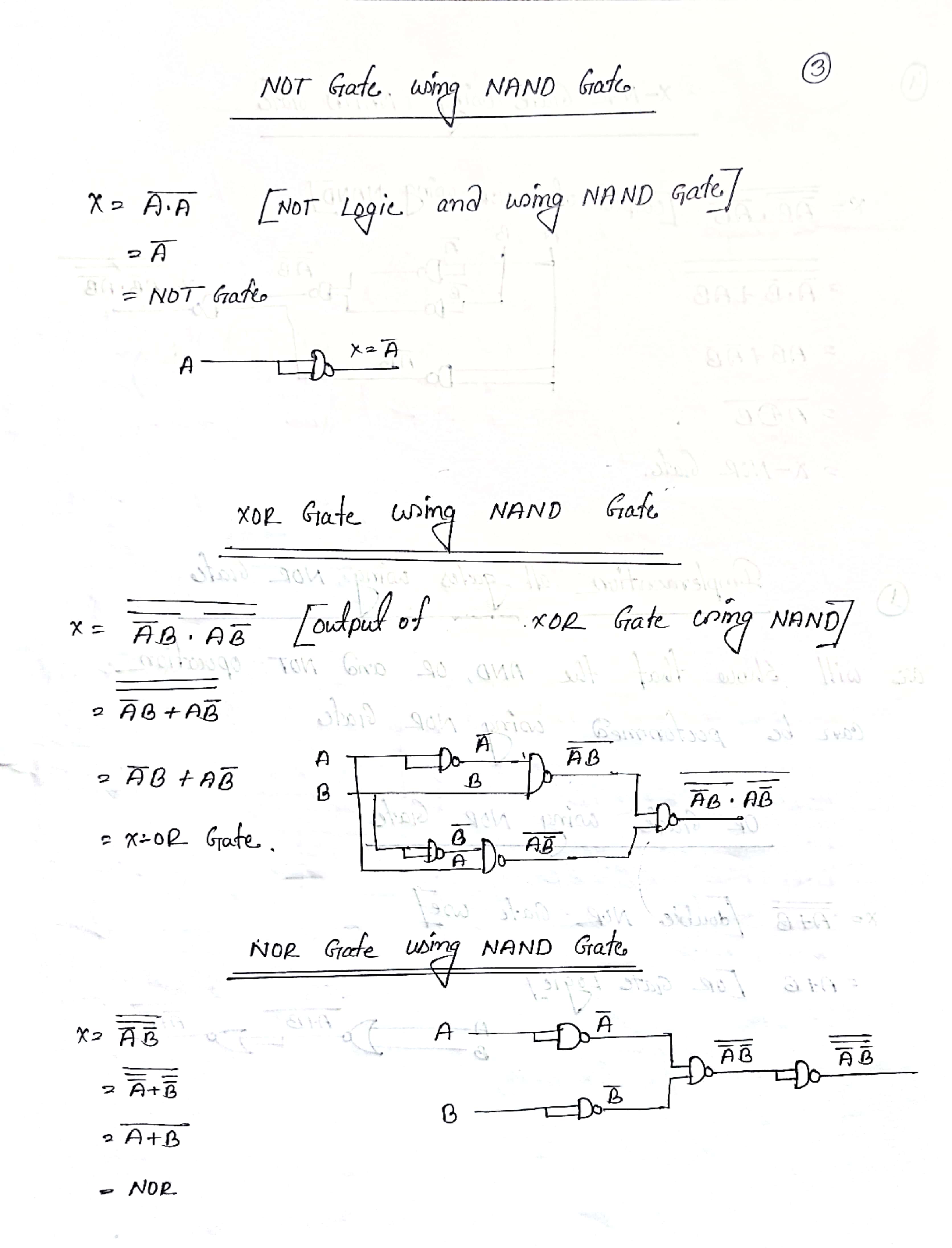
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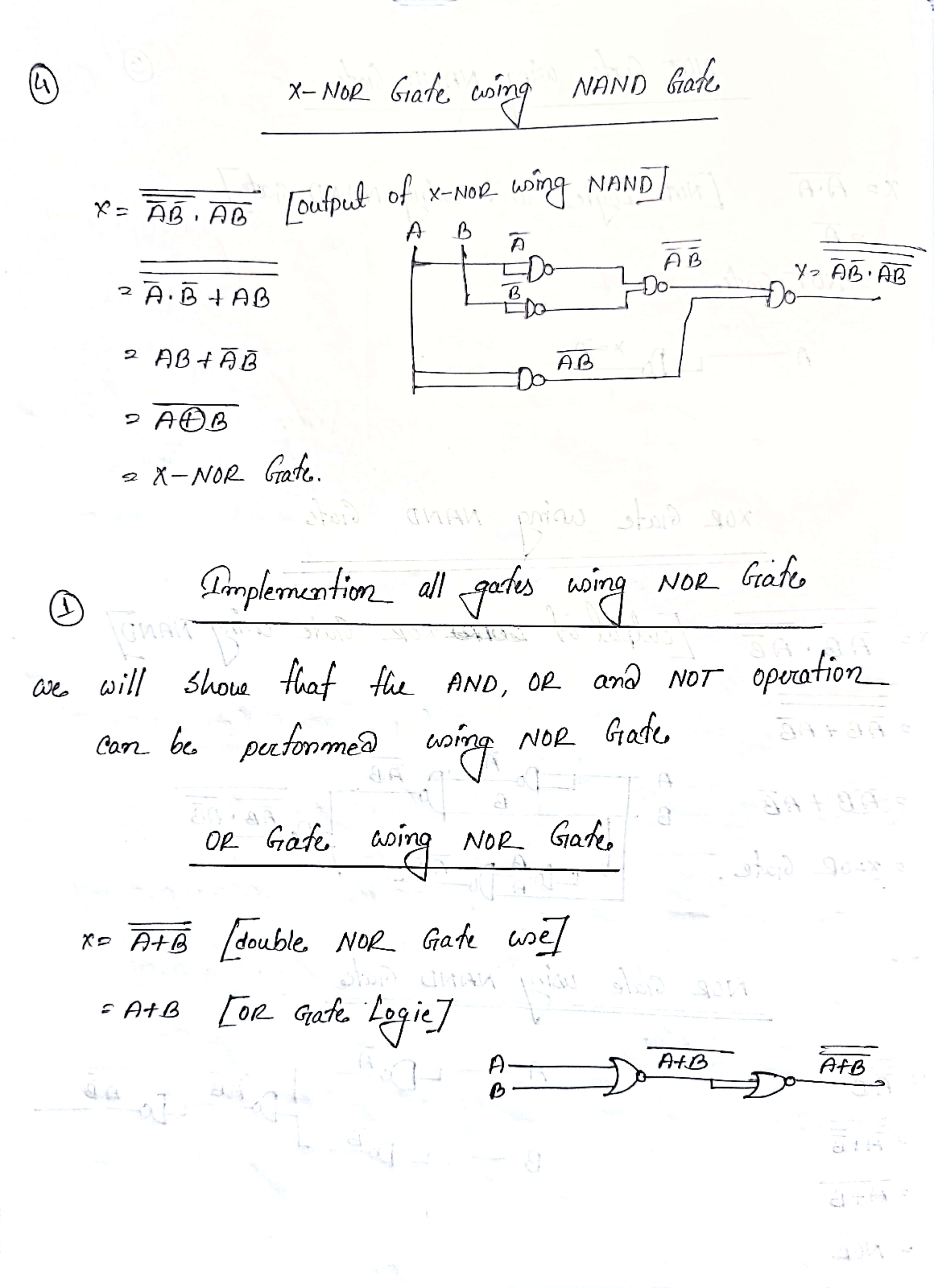
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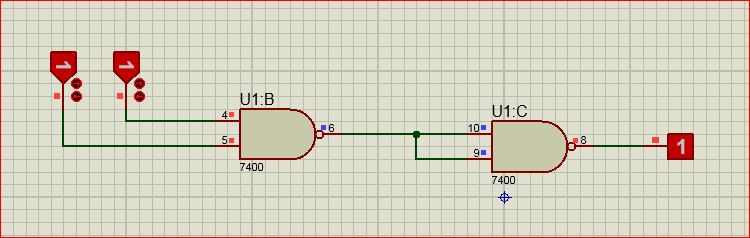
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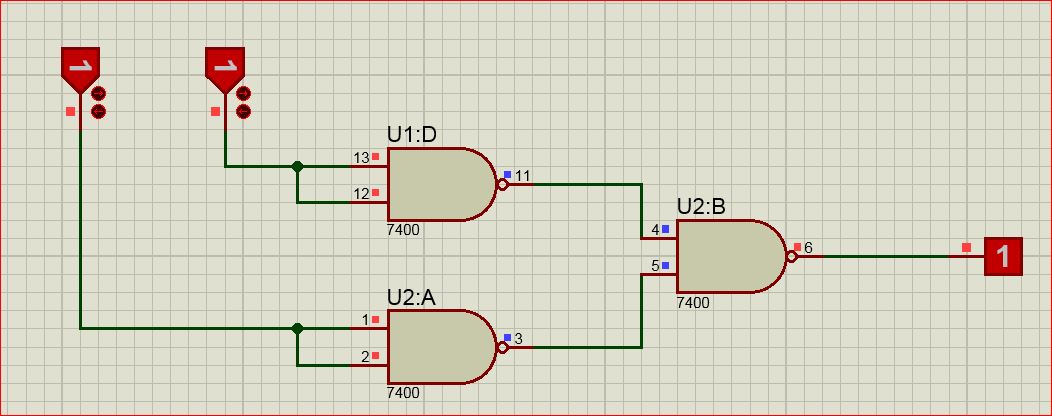




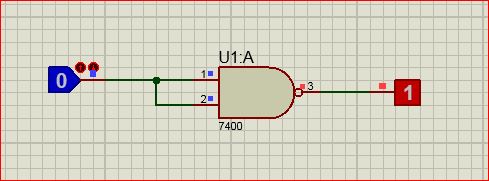




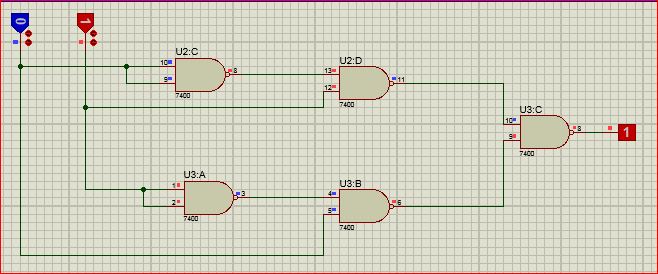
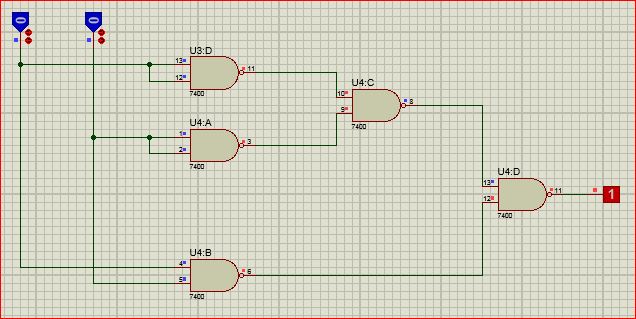
 Picture of AND Gate Using NAND Gate



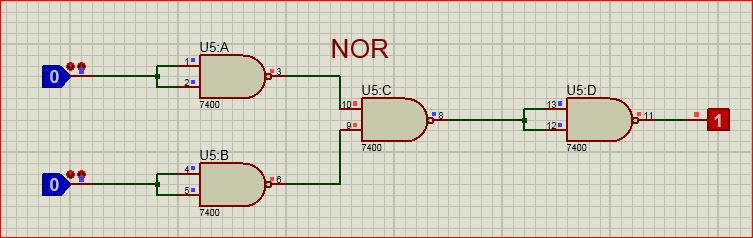
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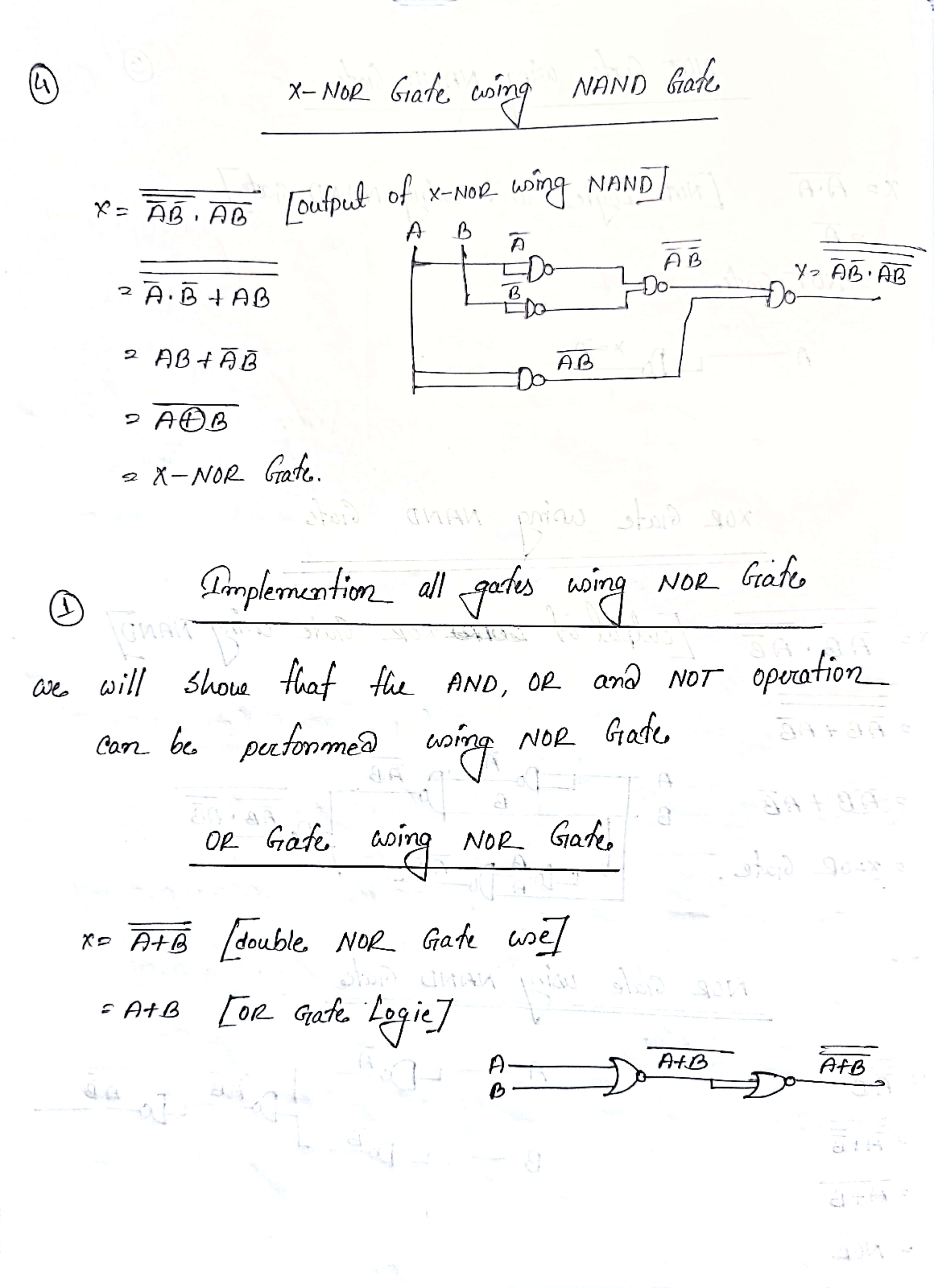


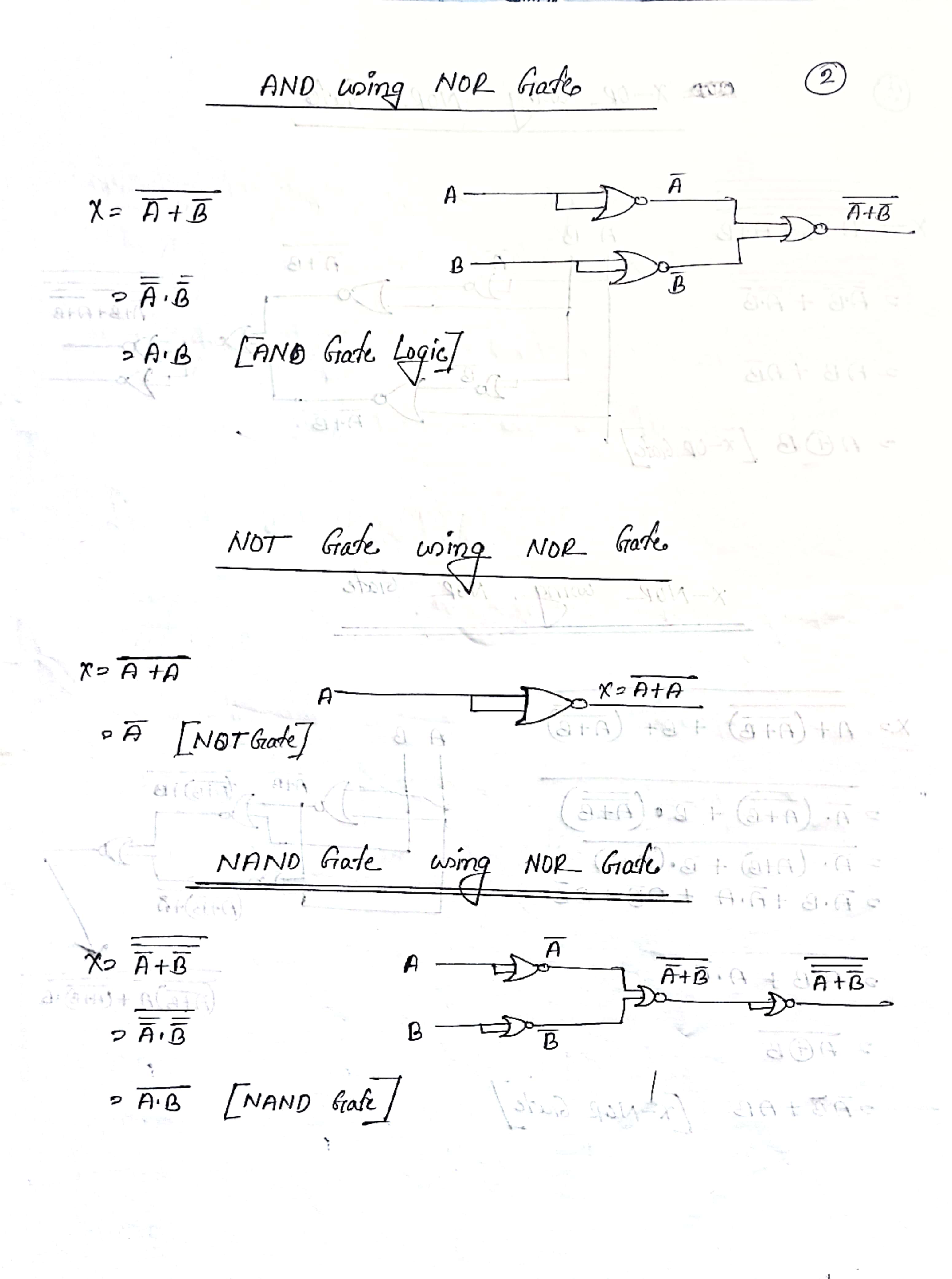
Picture of NOT Gate Using NAND Gate

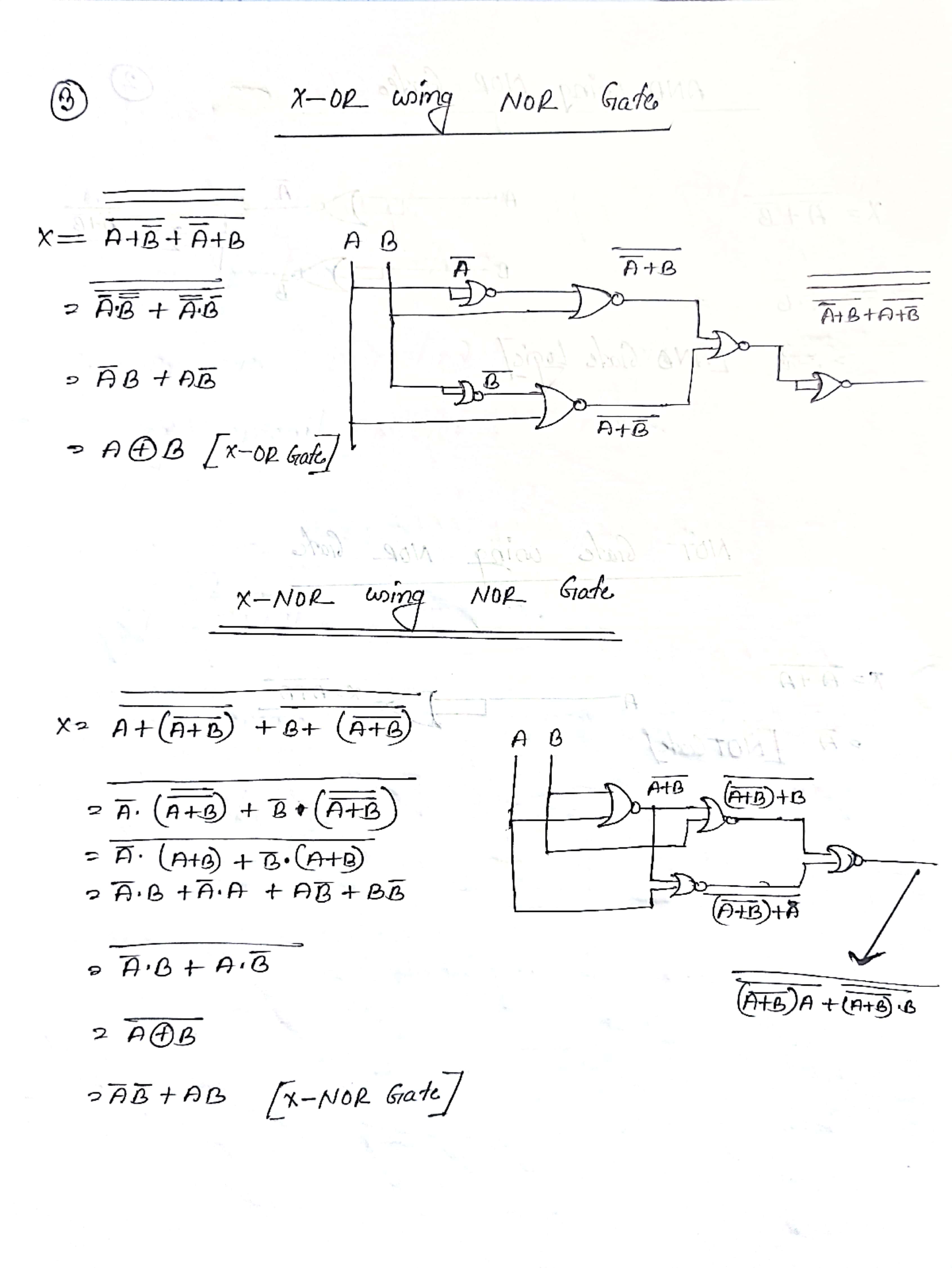
 Picture of X-OR Gate Using NAND Gate

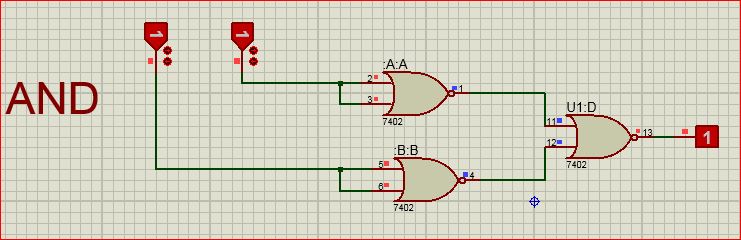
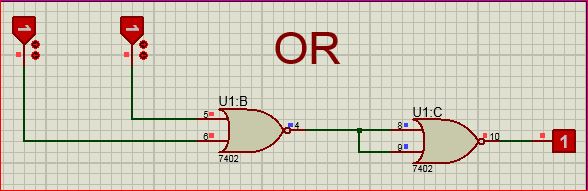
Picture of X-NOR Gate Using NAND Gate

Picture of NOR Gate Using NAND Gate 

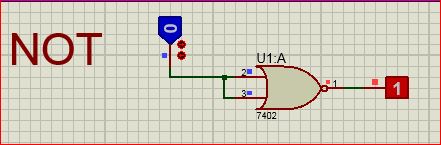


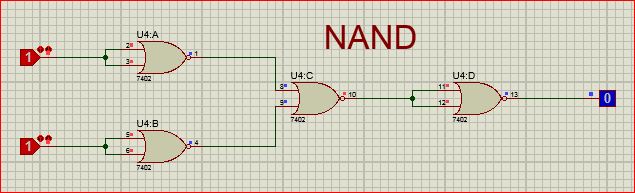




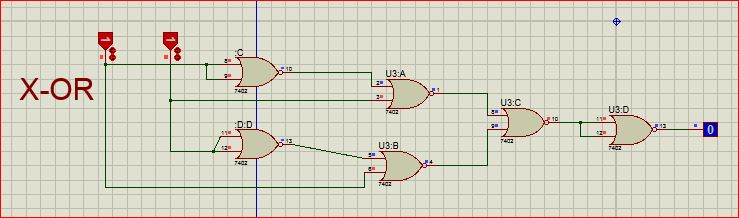
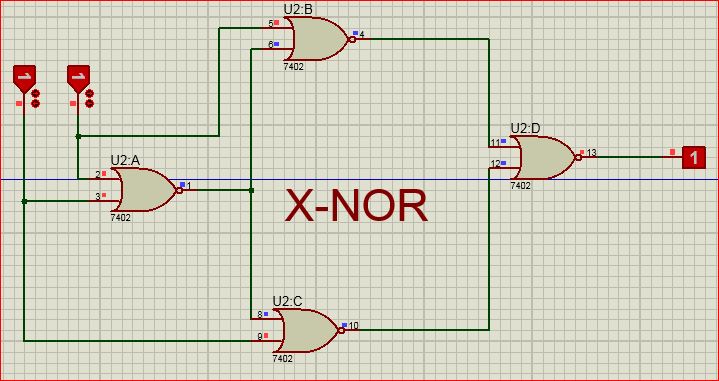
 Picture of AND Gate Using NOR gate

Picture of OR Gate Using NOR gate



 Picture of NOT Gate Using NOR gate

Picture of NOT Gate Using NOR gate

 Picture of X-OR Gate Using NOR gate

Picture of X-NOR Gate Using NOR gate

